**Experimental Evaluation of Modified Anderson PUF:**

We instantiated 90 instances of the design to generate a 90 Bit signature. We evaluate the design using virtex-5 FPGA’s on SASEBO G2 Board. The Board houses a Xilinx Virtex-5 (XC5VLX30 – FFFG324). A total of 19200 LUT cells are available and approximately a quarter of which can be used in shift register mode which gives ~ 4800 LUTs. The Board has a Xilinx Platform Connector Which we use to Communicate the PUF Signature to a connected PC. We clock the PUF using the 21 MHz clock signal available on the Board.

In addition to comparing PUF signatures across different signatures across different FPGA chips, we can also implement a PUF multiple times on a single chip, each time in a different region of the chip. Naturally, we expect that any two FPGA chips should differ more than any two regions on a single chip. Consequently, if PUF signatures for different regions on a single chip are subsequently unique. We have convincing evidence that signatures between chips will be at least unique following this reasoning in addition to comparing PUF signatures in virtex-5 chips. We investigated 4 PUF implementations one implementation in each of the 4 regions. PUF placement was constrained to regions using range constraints provided to Xilinx synthesis tool.

To analyze signature uniqueness, we consider the hamming distance between all PUF pairs producing (4\*3)/2 = 6 data points. A probability Histogram of such distances is shown. If logic-0 and logic-1 were equally probable one would expect the distribution to be clustered around an expected value of 45 bits. The average between any two pairs is 43 which is almost equal to 45.

We find the data points by combinations: Any two pairs taken from a set of numbers n is defined by nC2 which nothing is but

n!/(n-2)!2! which simplifies to

(n\*(n-1))/2

We plot the graph by finding the hamming distances and the density which is nothing but probability of the Hamming Distance occurring on the data point.